REMARKS

Reconsideration of the application is respectfully requested.

This amendment amends claims 1-9, 12-16, 18, 21-23, 30-31, 34-37, 40-44, and 54-57; no new claims have been added. No new matter has been added as the amendments are supported in the Specification as filed, for example, at page 6, paragraph 12.

Beginning with page 2 of the Office Action, the objections to Figs. 3 and 4 have been noted, and a proposed drawing correction is submitted here.

Regarding the Specification, the inconsistency regarding the "bus slave controller" has been corrected. In addition, the labeling of the memory controller has been reviewed and is deemed to be correct. There are two types of memory controllers referred to in the Specification, one being the memory controller 270 and another being the memory controller 430. However, in some cases, either the memory controller 270 or the memory controller 430 is the appropriate one to use. Therefore, in the interest of conciseness, the Specification refers to "memory controller 270/430". Therefore, further corrections are not believed to be necessary.

Additional corrections have been made for clarifying inconsistencies in the Specification regarding the signal 328.

The rejection under 35 U.S.C. §112, first paragraph is now moot as the allegedly violating claims have been canceled.

Turning now to the rejections under 35 U.S.C. §112, second paragraph, it is believed that the amendments here adequately address these issues.

Turning now to the art rejection, claim 1 has been amended to overcome anticipation by U.S. Patent No. 6,370,661 issued to Miner ("Miner"). It is submitted that Miner does not disclose, nor does it or another art reference cited by the Examiner suggest that Miner be modified into the system recited in claim 1, where a bus connects the processor to a bus slave controller, and wherein the bus slave controller is to

provide the processor access to the random access memory, and that the processor is to control the memory test engine via the bus and the bus slave controller.

Turning now to claim 16, this claim recites a method that has also been amended to overcome anticipation by Miner. Miner does not teach or suggest such a method for accessing and testing using separate bus slave controllers and separate memory testing engines.

Turning now to claim 30, this claim has also been amended to overcome the anticipation rejection in view of Miner, by reciting the capability in the form of instructions executed by a machine, of accessing a memory associated with an ASIC via a utility bus slave (UBS) controller over a bus. A memory test engine (MTE) is configured by writing to the UBS controller over the bus. The instructions are further capable of processing a signal from the MTE that a test of the memory is complete. Miner does not teach or suggest such a capability for accessing a memory via a UBS controller over a bus, and configuring the memory test engine by writing to the UBS controller over the bus.

As to claim 44, this claim has been rewritten to recite a means for simultaneously testing each of a plurality of memories, means for initiating the testing, and means for giving the initiation means access to each of the memories and access to the testing means. As these claim limitations are in the form of a means plus function, as allowed in 35 U.S.C. §112, paragraph 6, they are understood as referring to the structure disclosed in the Specification that is necessary to perform the recited functions, and an equivalent to such structure. Thus, for example, the means for simultaneous testing of each memory may correspond to multiple instances of the MTE 200 or, in the alternative, a single instance of MTE 410 (see Figs. 2 and 4, respectively). The means for initiating the testing may correspond to the CPU 211 (Fig. 2) or, in the alternative, to PCLM 400 (Fig. 4). Finally, the means for giving the initiation means access to each memory and access to the testing means may correspond to, in the case of Fig. 2, a bus 220, followed by a translator 230, a master bus controller 240, and multiple instances of bus slave controller 250. In the alternative, referring now to Fig. 4, the means for giving the initiation means access to the memories, as well as access to the testing

means may be an instance of a data transfer engine (DTE) 420 which may be used in situations where the utility bus system as shown in Fig. 2 is not used. Miner does not disclose the structural components of such an apparatus, and neither does it teach nor suggest modifications that would be deemed an equivalent under 35 U.S.C. §112, paragraph six.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

CONCLUSION

In sum, a good faith attempt has been made to explain why the rejection of the claims is improper, and how the claims are believed to be in condition for allowance. A Notice of Allowance referring to claims 1-9, 12-16, 18-23, 26-31, 34-37, 40-44, 47-48, and 54-57, as amended here, is therefore respectfully requested to issue at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: March 12, 2004

By _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on March 12, 2004.

Margaux Rodriguez *March 12, 2004*